12.2 A 40-to-44Gb/s 3× Oversampling CMOS CDR/1:16 DEMUX

Nikola Nedovic[1], Nestoras Tzartzanis[1], Hirotaka Tamura[2], Francis Rotella[1], Magnus Wiklund[1], Yuma Mizutani[3], Yusuke Okaniwa[3], Tadahiro Kuroda[3], Junji Ogawa[2], William Walker[1]

[1]Fujitsu Laboratories of America, Sunnyvale, CA
[2]Fujitsu Laboratories, Kawasaki, Japan
[3]Keio University, Yokohama, Japan

SONET OC-768 FEC CDRs have been successfully implemented in SiGe BiCMOS and compound semiconductor technologies [1-4], and an experimental 40Gb/s CDR/1:2 DEMUX has also been demonstrated in CMOS [5]. In this paper, an inductorless 40 to 44Gb/s CMOS CDR with an integrated 1:16 DEMUX and BER tester (BERT) is fabricated in a 10M triple-well 90nm 1.2V CMOS ASIC process. 3× oversampling and a digital CMOS back-end enable high-frequency jitter tracking while the CDR loop tracks low-frequency jitter. The chip consumes 0.91W, compared to 7.5W for a SiGe implementation with the same 1:16 DEMUX capability [3].

The receiver (Fig. 12.2.1) comprises a data delay line, a 24-phase 10GHz VCO, six 1:8 DEMUX blocks, a digital CDR back-end unit, a charge pump, and a loop filter. A JTAG TAP and an on-chip BERT circuit simplify setup and testing. No reference clock is used, the CDR acquires frequency lock from the 40Gb/s differential input data, $din/\overline{din}$. The output is the 2.5GHz recovered clock, *rclk,* and 16×2.5Gb/s recovered data, *dout*[15:0].

The data delay line, a loaded Z_0 = 85Ω U-shaped coplanar differential transmission line (Fig. 12.2.2) outputs 6 samples of the input data stream delayed from each other by UI/6. Each of the 7 segments is loaded with 4 binary-weighted varactors for tuning the delay, and a shunt resistor to equalize series and parallel losses, which also minimizes ISI. The capacitive load due to varactors and 6 decision circuits reduces the effective impedance of the line to 35Ω, hence, the use of a 35Ω termination. Increasing the effective impedance closer to 50Ω would require a narrow trace to obtain a large raw Z_0, resulting in unacceptable series losses. The transmission line is optimized using an EM simulator.

The 24-phase 10GHz distributed VCO is based on continuous wave propagation [6]. It consists of 12 transmission line segments similar to the data line, each loaded with a regenerative negative g_m circuit, a bank of 4 digitally controlled varactors for coarse tuning, and a varactor with an analog *Vctrl* input for fine frequency control. Each segment shifts the phase 15°, or 1/6 UI. The 6 adjacent clock phases on top of the VCO and their complements drive the 6 DEMUX blocks.

A 1:8 DEMUX block receives data and clock inputs, samples every other input bit, and generates eight 2.5Gb/s outputs. Each DEMUX block contains 2 decision circuits that sample input data at both edges of the clock, a 2:4 5Gb/s DEMUX, a 4:8 2.5Gb/s DEMUX, and a 1:4 frequency divider. The decision circuit (Fig. 12.2.3) is based on the circuit presented in [7], and improved for an aperture of 0.1UI, which is critical for the performance of the CDR. The decision circuit consists of a sampler/latch, a regenerative sense amplifier, and a 2-stage buffer. The sampler/latch features 2 clocked PMOS transistors, *p1* and *p2* for fast shut-off of the input differential pair. Negative feedback *n5-n8* resets the internal nodes and the output of the sense amplifier to the common voltage level when the clock is low (input latch transparent) in order to reduce the effect of the previous decisions on the current sample. When the clock switches high, the voltage difference on $in/\overline{in}$ is amplified by transistors *n1-n4*. Following the decision circuit, a 5Gb/s 1:2 DEMUX and a 2.5Gb/s 4:8 DEMUX are implemented using latches. 1:4 frequency dividers in each DEMUX provide quadrature phases of a 5GHz clock to synchronize the 2 incoming 180°-separated 10Gb/s data streams from the decision circuit. All circuits are implemented using standard CML logic without inductors, allowing for compact layouts. The 48 2.5Gb/s samples from the 6 DEMUXs are fed under the data line, then converted from CML levels to single-ended CMOS levels.

The 5-stage pipelined digital CDR (Fig. 12.2.4) receives 48 samples, *s*[47:0], and outputs 2.5Gb/s recovered 16b data and clock, *dout*[15:0] and *rclk*, and sends the control signals, *up, up3, dn, dn3, frup, frdn*, to the charge pump to track the phase and frequency. It first detects the location of transitions in the input samples, retaining the previous transitions if none are found. By comparing the current phase with the previous phase in 4UI groups, the CDR can detect the direction of the change of phase displacement. Two one-hot 3b pointers *ptr_m*[2:0] and *ptr_l*[2:0] and a 9-entry 16b elastic FIFO allow for phase tracking of up to ±1.5UI in steps of UI/3. While in lock, the CDR tracks the input phase by asserting a combination of *up, up3, dn,* and *dn3* signals that code the FIFO position, thus making the charge pump current a linear function of the phase error. If a FIFO overflow is detected, an out-of-lock condition is reached, and *frup* or *frdn* is asserted for frequency acquisition.

The charge pump and loop filter receive *up, up3, dn, dn3, frup, frdn* inputs from the digital CDR and output *vctrl* to the VCO. The charge pump uses digitally tunable reference current for external control of loop gain. It operates in the μA range to enable use of on-chip capacitors in the loop filter. To achieve sufficient output resistance, the charge pump has cascode current mirrors in each branch. The cascode current mirrors are self-biased to maximize the linear range of the output voltage and the available tuning range of the VCO. The loop filter is implemented using polysilicon resistor and thick oxide MOS capacitors to minimize gate leakage.

Circuit blocks are simulated using SPICE and Verilog, and characteristics are abstracted into event-triggered Simulink time-domain models. Non-idealities such as the VCO jitter and phase deviation, sampler aperture, and data-line losses are all modeled. Using event-triggered simulation resulted in simulation speeds exceeding 10000symbols/s. allowing validation of the jitter tolerance mask in a few hours.

The receiver macro size is 0.8×1.8mm^2 (Fig. 12.2.7). The on-chip BERT, accessible via a scan interface, is capable of checking 2^{31}-1 and 2^{15}-1 PRBS and counting loss-of-lock events. A 40Gb/s PRBS generator driven by an external phase-modulated clock supplies data with sinusoidal jitter to the DUT. The CDR successfully locks between 39.96 and 44.22Gb/s. The phase noise of the recovered clock is shown in Fig. 12.2.5. Jitter tolerance for BER<10^{-12}, measured with both on-chip and off-chip BERT using the 2^{31}-1 PRBS pattern, is plotted on top of the ITU-T G.8251 mask in Fig. 12.2.6. Power consumption is measured to be 0.84W from the 1.4V analog supply, and 70mW from the 1.34V digital supply (also including test logic), 0.91W total.

References:
[1] M. Megheli, A.V. Rylyakov, S.J. Zier, et al, “A 0.18μm SiGe BiCMOS Receiver and Transmitter Chipset for SONET OC-768 Transmission Systems,” *ISSCC Dig. Tech. Papers*, pp. 230-231, Feb., 2003.
[2] A. Koyama, T. Harada, H. Yamashita, et al, “43Gb/s Full-Rate-Clock 16:1 Multiplexor and 1:16 Demultiplexor with SFI-5 Interface in SiGe BiCMOS Technology,” *ISSCC Dig. Tech. Papers,* pp. 232-233, Feb., 2003.
[3] A. Ong, S. Benyamin, V. Condito, et al, “A 40-43Gbp/s Clock and Data Recovery IC with Integrated SFI-5 1:16 Demultiplexor in SiGe Technology,” *ISSCC Dig. Tech. Papers* , pp. 234-235, Feb., 2003.
[4] J. Yen, M.G. Case, S.Nielsen, et al, “A Fully Integrated 43.2Gb/s Clock and Data Recovery and 1:4 DEMUX IC in InP HBT Technology,” *ISSCC Dig. Tech. Papers* , pp. 240-241, Feb., 2003.
[5] J. Lee and B. Razavi, “A 40Gb/s Clock and Data Recovery Circuit in 0.18μm CMOS Technology,” *ISSCC Dig. Tech. Papers* , pp. 242, Feb., 2003.
[6] N. Tzartzanis and W. Walker, “A Reversible Poly-Phase Distributed VCO,” *ISSCC Dig. Tech. Papers* , pp. 596-597, Feb., 2006.
[7] Y. Okaniwa, H. Tamura, M. Kibune, et al, “A 0.11μm CMOS Clocked Comparator for High-Speed Serial Communications,” *Symp. on VLSI Circuits*, pp. 198-201, Jun., 2004.

 1-4244-0852-0/07/$25.00

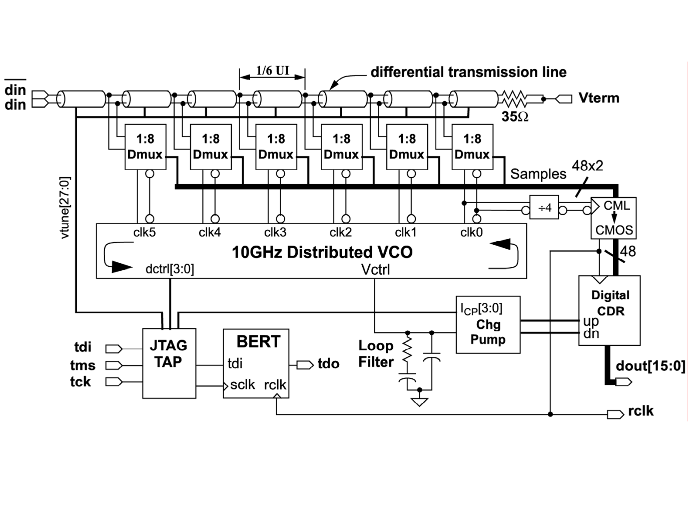

Figure 12.2.1: Block diagram of the 40Gb/s CDR.

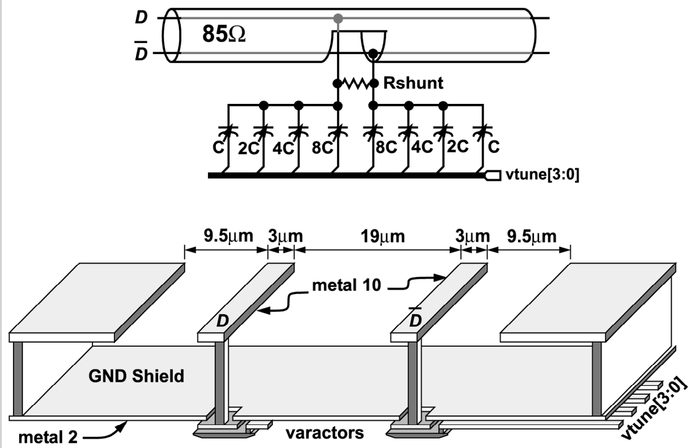

Figure 12.2.2: Data delay line segment schematic and cross-section.

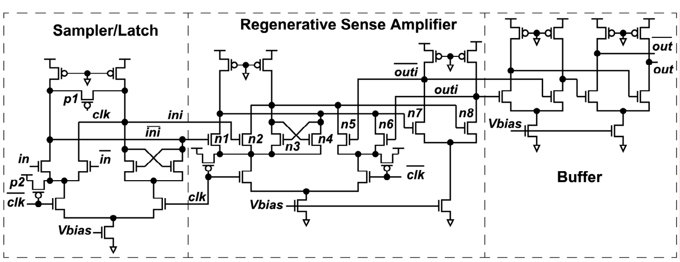

Figure 12.2.3: Front-end decision circuit.

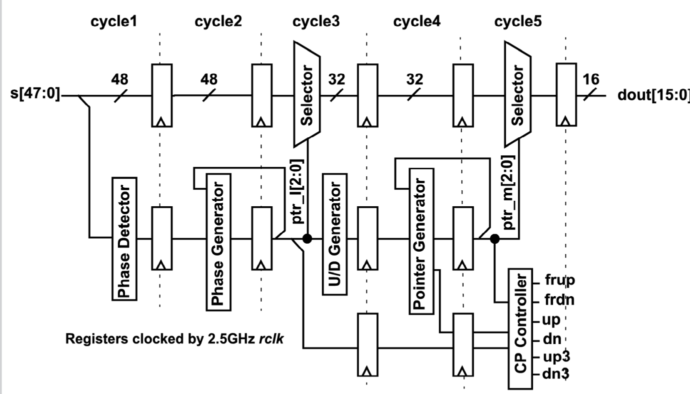

Figure 12.2.4: Pipeline diagram of digital CDR.

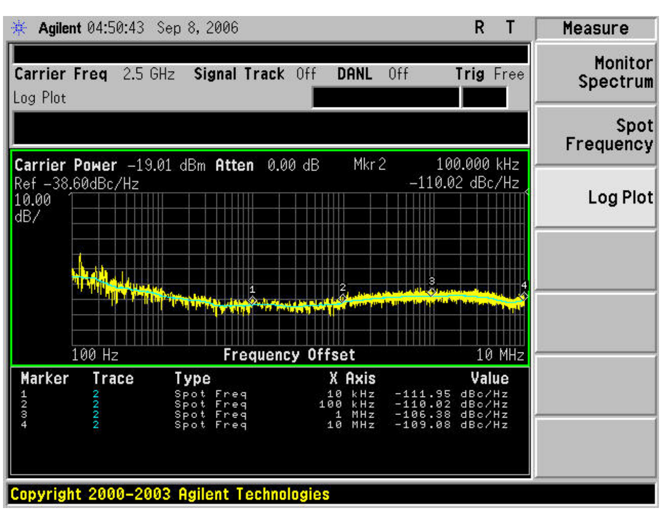

Figure 12.2.5: Phase noise of the recovered clock.

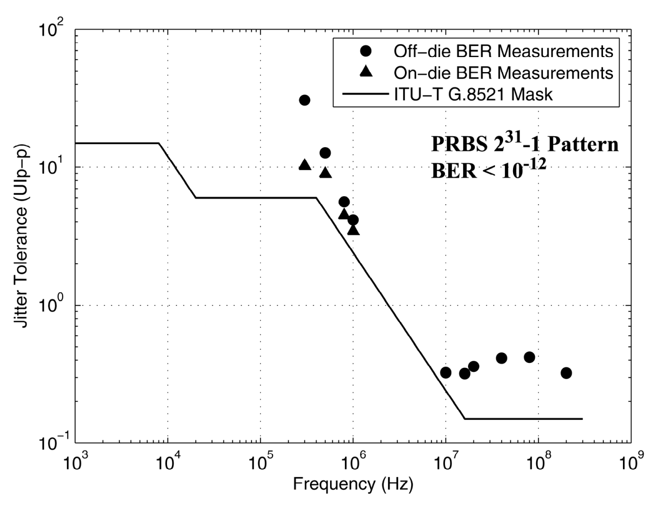

Figure 12.2.6: Measured jitter tolerance.

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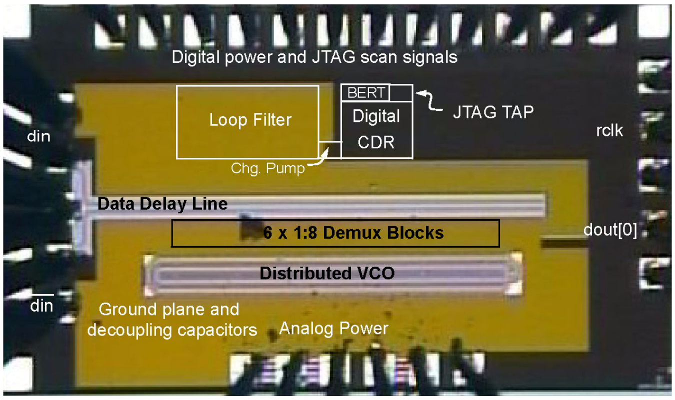

Figure 12.2.7: Die micrograph.